	Document ID	U	Title	Current OR
1	US 5909572 A	☐	System and method for conditionally moving an operand from a source register to a destination register	712/226
2	US 5781457 A	☐	Merge/mask, rotate/shift, and boolean operations from two instruction sets executed in a vectored mux on a dual-ALU	708/231
3	US 5680161 A	☐	Method and apparatus for high speed graphics data compression	345/531
4	US 5625374 A	☐	Method for parallel interpolation of images	345/639
5	US 5594437 A	☐	Circuit and method of unpacking a serial bitstream	341/67
6	US 5579253 A	☐	Computer multiply instruction with a subresult selection option	708/625
7	US 5487159 A	☐	System for processing shift, mask, and merge operations in one instruction	712/223
8	US 5465374 A	☐	Processor for processing data string by byte-by-byte	711/219
9	US 5426783 A	☐	System for processing eight bytes or less by the move, pack and unpack instruction of the ESA/390 instruction set	712/225
10	US 5423010 A	☐	Structure and method for packing and unpacking a stream of N-bit data to and from a stream of N-bit data words	341/60
11	US 5408670 A	☐	Performing arithmetic in parallel on composite operands with packed multi-bit components	712/16
12	US 5390135 A	☐	Parallel shift and add circuit and method	708/518
13	US 5268995 A	☐	Method for executing graphics Z-compare and pixel merge instructions in a data processor	345/422
14	US 5187679 A	☐	Generalized 7/3 counters	708/706
15	US 5168571 A	☐	System for aligning bytes of variable multi-bytes length operand based on alu byte length and a number of unprocessed byte data	712/210
16	US 5054957 A	☐	Digital multiplier employing CMOS transistors	708/626
17	US 5016098 A	☐	Method and apparatus for graphics display data manipulation	345/422
18	US 4989168 A	☐	Multiplying unit in a computer system, capable of population counting	708/210
19	US 4903228 A	☐	Single cycle merge/logic unit	712/224
20	US 4771379 A	☐	Digital signal processor with parallel multipliers	712/42
21	US 4707800 A	☐	Adder/substractor for variable length numbers	708/714
22	US 4498177 A	☐	M Out of N code checker circuit	714/806
23	US 4418383 A	☐	Data flow component for processor and microprocessor systems	710/307

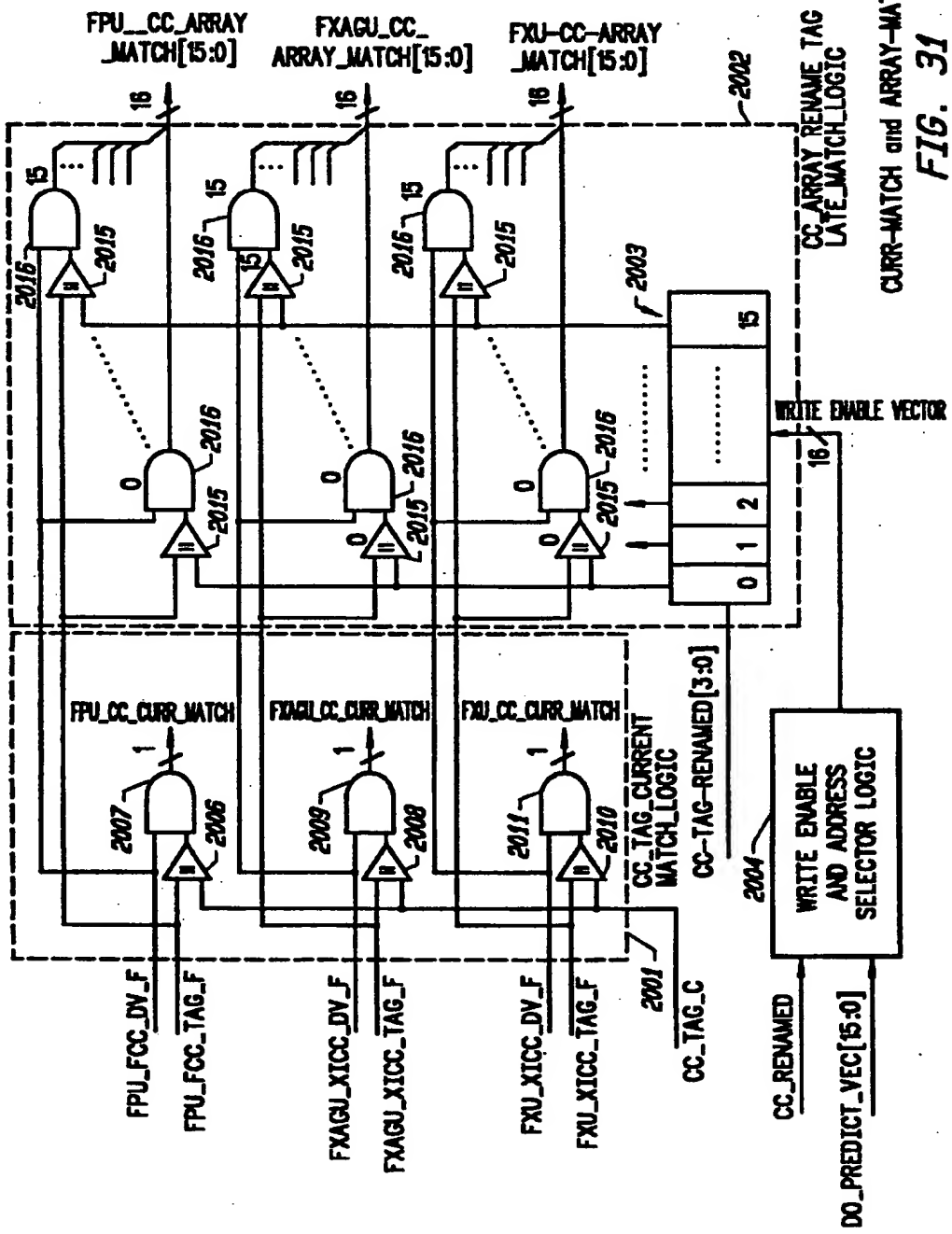
FPU_CC_ARRAY_MATCH[15:0]
FXAGU_CC_ARRAY_MATCH[15:0]
FXU-CC-ARRAY_MATCH[15:0]
CC_ARRAY RENAME_TAG LATE_MATCH_LOGIC
CURR-MATCH and ARRAY-MATCH logic
WRITE ENABLE VECTOR
FPU_CC_CURR_MATCH
FXAGU_CC_CURR_MATCH
FXU_CC_CURR_MATCH
CC_TAG_CURRENT MATCH_LOGIC
CC-TAG-RENAMED[3:0]
WRITE ENABLE AND ADDRESS SELECTOR LOGIC
FPU_FCC_DV_F
FPU_FCC_TAG_F
FXAGU_XICC_DV_F
FXAGU_XICC_TAG_F
FXU_XICC_DV_F
FXU_XICC_TAG_F
CC_TAG_C
CC_RENAMED
DO_PREDICT_VEC[15:0]

FIG. 31

	Document ID	U	Title	Current OR
24	US 4393468 A	☐	Bit slice microprogrammable processor for signal processing applications	708/518
25	US 4161784 A	☐	Microprogrammable floating point arithmetic unit capable of performing arithmetic operations on long and short operands	708/513
26	US 4139899 A	☐	Shift network having a mask generator and a rotator	712/224
27	US 3723715 A	☐	FAST MODULO THRESHOLD OPERATOR BINARY ADDER FOR MULTI-NUMBER ADDITIONS	708/709
28	US 3711692 A	☐	DETERMINATION OF NUMBER OF ONES IN A DATA FIELD BY ADDITION	708/210

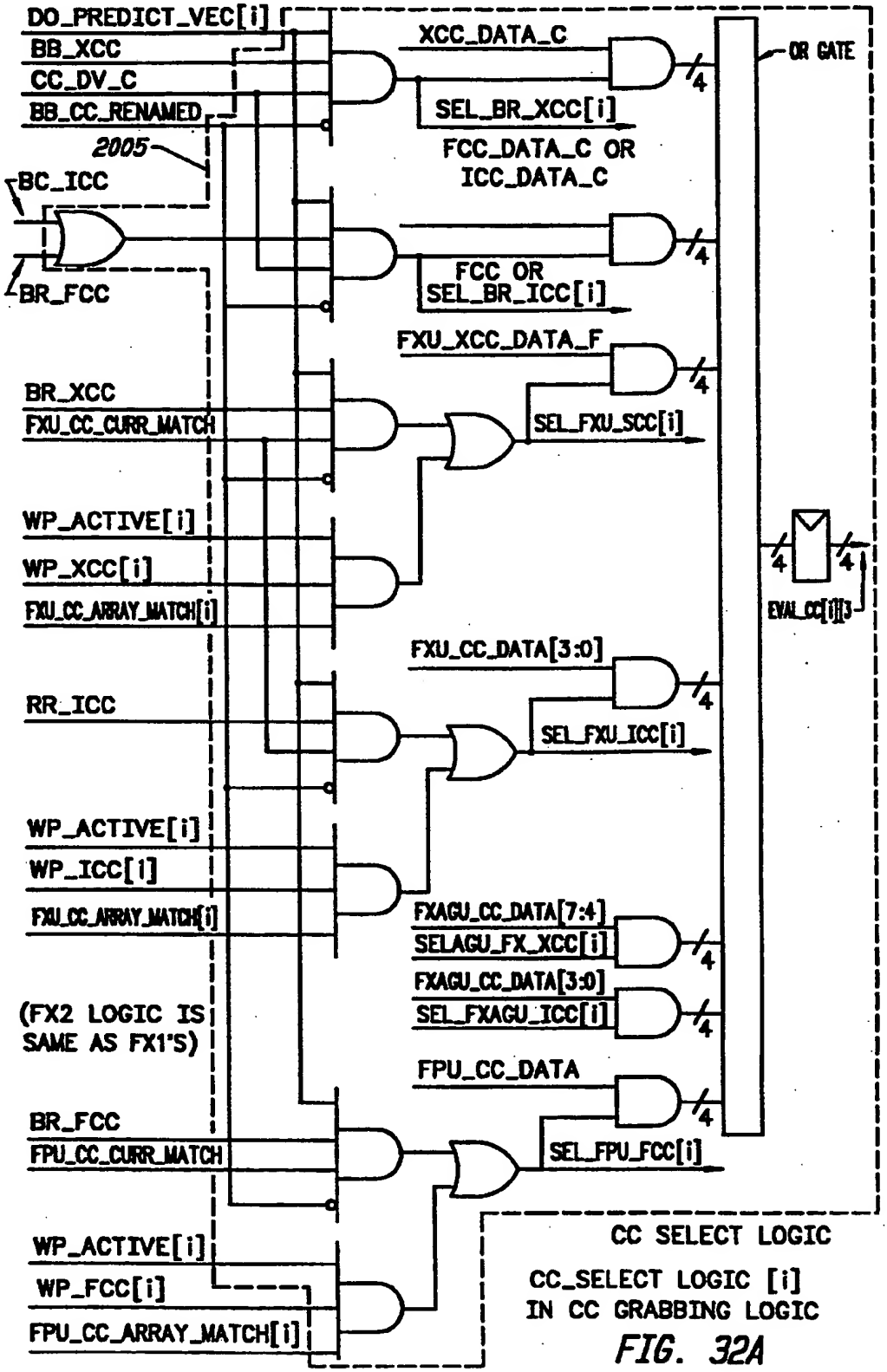
DO_PREDICT_VEC[i]
BB_XCC
CC_DV_C
BB_CC_RENAMED
2005
BC_ICC
BR_FCC
BR_XCC
FXU_CC_CURR_MATCH
WP_ACTIVE[i]
WP_XCC[i]
FXU_CC_ARRAY_MATCH[i]
RR_ICC
WP_ACTIVE[i]
WP_ICC[i]
FXU_CC_ARRAY_MATCH[i]
(FX2 LOGIC IS SAME AS FX1'S)
BR_FCC
FPU_CC_CURR_MATCH
WP_ACTIVE[i]
WP_FCC[i]
FPU_CC_ARRAY_MATCH[i]
XCC_DATA_C
SEL_BR_XCC[i]
FCC_DATA_C OR ICC_DATA_C
FCC OR SEL_BR_ICC[i]
FXU_XCC_DATA_F
SEL_FXU_SCC[i]
FXU_CC_DATA[3:0]
SEL_FXU_ICC[i]
FXAGU_CC_DATA[7:4]
SELAGU_FX_XCC[i]
FXAGU_CC_DATA[3:0]
SEL_FXAGU_ICC[i]
FPU_CC_DATA
SEL_FPU_FCC[i]
OR GATE
EVAL_CC[i][3]
CC SELECT LOGIC
CC_SELECT LOGIC [i]
IN CC GRABBING LOGIC

FIG. 32A